ABSTRACT

Processor instruction pipelines, which split the processing of individual instructions into several sub-stages and thus reduce the complexity of each stage while simultaneously increasing the clock speed, are typical features of RISC architectures. Operands required by the processing are read from a register file. Read-after-write access problems in the pipeline processing can be avoided by using a scoreboard that has an individual entry per address of the register file. Once an instruction enters the pipeline, a flag is set at the address of the destination address of this particular instruction. This flag signals that an instruction inside the pipeline wants to write its result to the respective register address. Hence the result is unavailable as long as the flag is set. It is cleared after the instruction process has successfully written the result into the register file. According to the invention, not only a single flag but the number of the pipeline stage, which currently carries the instruction that wants to write its result to a particular register file address, and the type of the respective instruction is stored in the corresponding scoreboard address for the particular instruction.